28.7 A 2/3 inch CMOS Image Sensor for HDTV Applications with Multiple High-DR Modes and Flexible Scanning

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Developing cost effective camera solutions for low-volume applications is a challenge. This paper describes an imager designed from a system-architectural point of view that fulfils this requirement.

The novelty of this 3T-CMOS imager can be found in its flexible scanning options, which are implemented while maintaining broadcast performance. This combination is enabled by using three SELECT and two RESET shift registers, whereas in standard imagers, only one SELECT and one RESET register are present.

The flexibility in scanning modes manifests itself in the choice of 1080 lines progressive or interlaced scanning, with enhanced DR modes and all the while maintaining (digital) correlated double sampling (CDS) at arbitrary exposure times.

The imager is designed for use in a 3-chip application, which puts additional demands on the timing and linearity of the devices. Each imager has 1920(H)×1080(V) active pixels and 2 on-chip 12b analog-to-digital converters. Figure 28.7.1 shows the block diagram of the sensor. This imager supports up to 90 progressive frames per second and 180 interlaced fields per second. Experiments where performed up to 120 progressive frames per second, or 296Mpixels/s.

The standard 3T-pixel architecture typically has a low signal-to-noise ratio due to the large reset or kT/C noise. Many techniques for reset noise reduction are based on a soft-reset method [1-3]. But the remaining image lag after soft reset is not acceptable for broadcast applications.

The other method of noise reduction is to implement CDS as it was originally supposed to be [4]: "sample the pixel value at the start of the integration cycle, sample the pixel value at the end of the integration time and subtract the two values", thereby effectively eliminating kT/C noise. Normally, like in a CCD operating at a high frequency, the $1/f$ noise is also suppressed with CDS. But, the effect of CDS on the overall noise level in a CMOS imager is very much dependent on the time between the two samples of the CDS operation. The dominant $1/f$ noise source in a CMOS imager is located in the pixel and with digital CDS one might expect a large value of $1/f$ noise to remain because of the long time between the two samples. But the advantage of the CMOS imager can be found in the multiplexing of the pixel outputs. The column readout de-correlates the low-frequency noise from pixel to pixel, and after CDS the $1/f$ noise only increases the overall noise at the pixel level, not at the column or row level.

Several architectures have been devised [5-8] to enhance the DR of CMOS image sensors. The new imager supports both temporal and spatial sub-sampling methods to increase its DR.

The temporal sampling method is best described as triple sampling with arbitrary timing. The three samples for each pixel represent the black reference level, the video level and an intermediate video level, and can be used to generate a composite image. Pixels that are saturated are extrapolated from the intermediate pixel value.
The spatial sampling method is a combination of horizontal and/or vertical sub-sampling. When reducing horizontal resolution for increased DR, all the even pixels have nominal exposure times and all the odd pixels have reduced exposure times. The odd pixels are readout through the odd ADC and the even pixels are readout through the even ADC as shown in Fig. 28.7.2. To increase DR at the cost of vertical resolution, the odd rows have nominal exposure times and even rows have reduced exposure times. The two reset registers control the different exposure times.

A noise level of 11.5e^- (4e^- pixel only) was obtained at 1080 lines/frame, interlaced scan, 60 fields per second; and a saturation level of more than 15ke^- per pixel was measured. The data rate of the sensor was designed to be 2.7Gbps and is measured to be 3.6Gbps as shown in Fig. 28.7.3.

CDS and the different DR-enhancement modes are enabled through the use of three SELECT shift registers and two RESET shift registers, all on-chip. Figure 28.7.4 shows the architecture of the vertical timing control.

As an example, normal operation for an arbitrary exposure time contains the following timing:

- SELECT 1 addresses the m-th row – in each pixel the video and black information has to be read;
- RESET 1 resets the n-th row and, depending on the application, the m-th row could also be reset at the same time;
- SELECT 2 addresses the n-th row that has been reset – for each pixel the black information is read.

Only in the case of nominal exposure are m and n the same. An external DDR-SDRAM frame-store aligns the black information from the pixels in the n-th row with the video information from the pixels in the n-th row to enable digital CDS.

In present day camera technology there is still a need for progressive and interlaced scanning. The choice between the two modes is realized by the external inputs of the shift registers, which are used to load an arbitrary pattern (token) into them. These patterns are clocked peristaltically with the speed and direction externally chosen.

Figure 28.7.5 shows measurements of the shot-noise transfer curves for both progressive (lower trace) and interlaced (upper trace) modes of operation. The zone chart in Fig. 28.7.6 shows the correct suppression of aliasing at the field sample frequency. The overall performance of the imager is summarized in Fig. 28.7.3. Figure 28.7.7 shows the chip micrograph.

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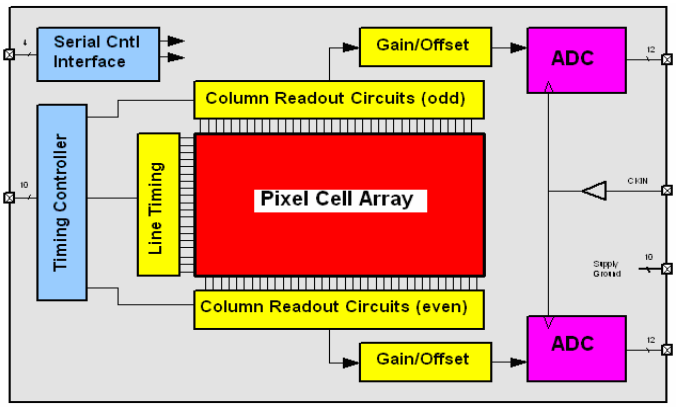

Figure 28.7.1: Block diagram of the imager.

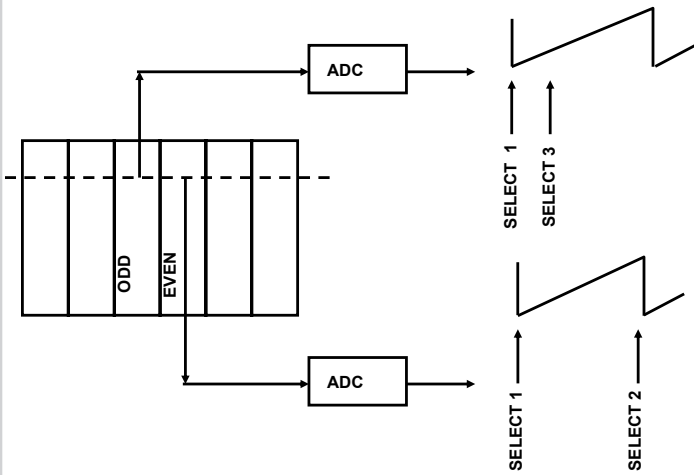

Figure 28.7.2: Horizontal high-DR readout.

Process	CMOS 0.18µm 1P4M
Supply Voltages	3.3V and 1.8V
Chip Size	155mm^2
Number of effective pixels	1920(H) x 1080(V)
Pixel size	5µm x 5µm
Transistors per pixel	3T
Pixel Fill Factor (without micro-lens)	44%
Analog to Digital Conversion	2 12b ADCs
Max. frame rate; designed (accomplished)	180fld/sec (240fld/sec)
Max. bit rate; designed (accomplished)	2.7Gbps (3.6Gbps)
Photon response non-uniformity	<1%
Conversion gain (FD)	80µV/e$^-$
Dark current @ 333K	0.4nA/cm^2
FPN @ 333K 60fld/sec	17e$^-$
Temporal Noise, all contributors, 300K	11.5e$^-$
Temporal Noise, pixel only, 300K	4e$^-$
Sensitivity in Green (495nm to 573nm)	32ke$^-$/lux·sec
Saturation level	>15ke$^-$
Maximum Reachable Dynamic Range	116dB in interlaced mode 122dB in progressive mode
Power Dissipation	550mW @ 60fps

Figure 28.7.3: Performance summary.

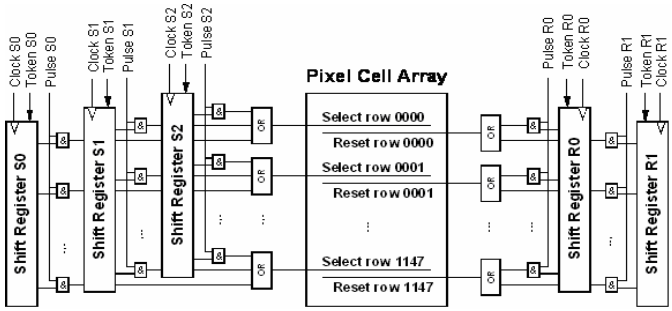

Figure 28.7.4: The vertical scanning control architecture.

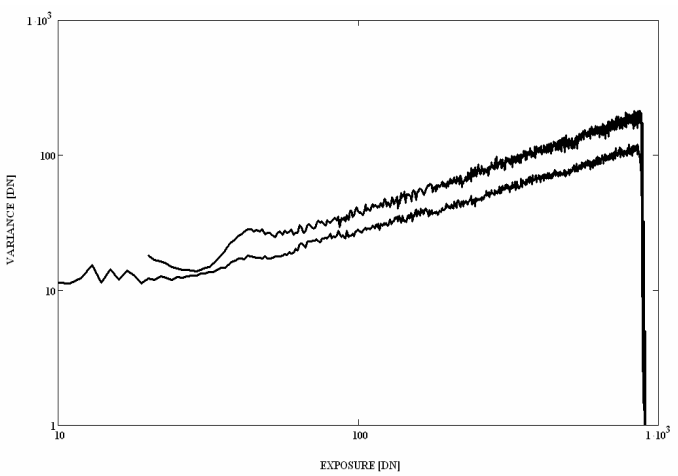

Figure 28.7.5: Photon shot-noise curves for progressive (lower trace) and interlaced (upper trace) scanning.

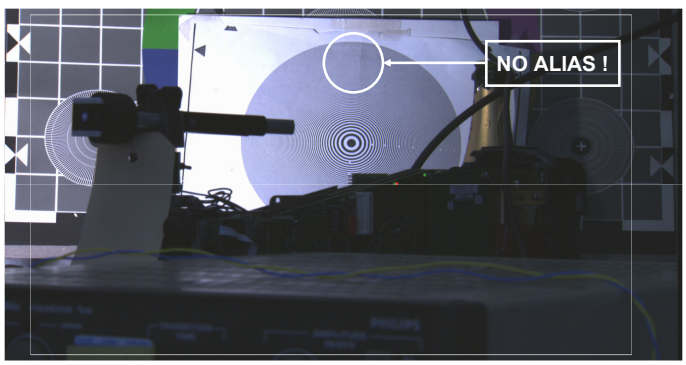

Figure 28.7.6: Interlaced image with zone chart in the background.

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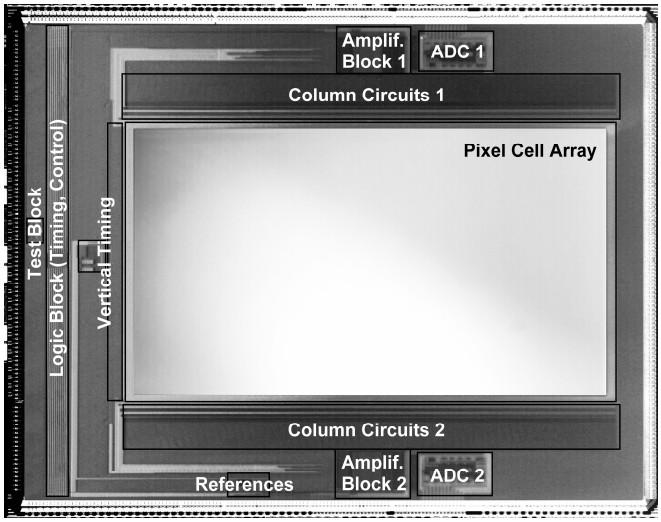

Figure 28.7.7: Chip micrograph.

